WHAT IS CLAIMED IS:

1. A method for performing an inverse discrete cosine transform (IDCT) on a plurality of input coefficients, the method for performing the IDCT comprising:

performing a first one directional (1D) IDCT resulting in a plurality of first 1D IDCT coefficients;

performing a second 1D IDCT resulting in a plurality of second 1D IDCT coefficients;

performing the first 1D IDCT and the second 1D IDCT including performing a first plurality of intermediate butterfly computations; and

rounding and shifting the plurality of second 1D IDCT coefficients resulting in a plurality of output coefficients.

2. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 1, wherein:

the step of performing the first plurality of intermediate butterfly computations including:

performing a plurality of intermediate multiplications resulting in a plurality of initial products; and

performing a plurality of intermediate additions.

3. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 2, wherein:

the step of performing a plurality of intermediate multiplications including:

multiplying input coefficients by a trigonometric constant producing an initial product; and

maintaining the initial product at no more than 16-bits.

4. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 3, wherein:

the step of maintaining the initial product at no more than 16-bits including shifting the initial product right a plurality of bits resulting in a shifted initial product; and

rounding the shifted initial product utilizing a round near positive (RNP) rounding scheme.

5. The method for performing the IDCT on the plurality of input coefficients as

claimed in claim 4, wherein:

the step of performing the first plurality of intermediate butterfly computations of the first 1D IDCT and the second 1D IDCT including performing a second plurality of intermediate butterfly computations simultaneously in parallel.

6. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 4, wherein:

the step of performing the intermediate butterfly computation of the first 1D IDCT and the second 1D IDCT including performing each intermediate butterfly computation in a single instruction.

7. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 3, wherein:

the step of maintaining the initial product at no more than 16-bits including rounding the initial product utilizing a round near positive (RNP) rounding scheme.

8. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 1, wherein:

performing the first and second 1D IDCT including rounding utilizing a RNP rounding scheme and not utilizing a rounding away from zero (RAZ) rounding scheme.

9. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 8, wherein:

the step of rounding and shifting including rounding utilizing a RAZ rounding scheme.

10. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 1, wherein:

the step of performing the intermediate butterfly computation of the first 1D IDCT and the second 1D IDCT including performing each intermediate butterfly computation in a single instruction.

11. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 10, wherein:

the step of performing the first plurality of intermediate butterfly computations of the first 1D IDCT and the second 1D IDCT including performing a second plurality of intermediate butterfly computations simultaneously in parallel.

12. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 1, wherein:

the step of performing the first plurality of intermediate butterfly computations including performing each intermediate butterfly computation in a single instruction.

13. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 12, wherein:

the step of performing the first plurality of intermediate butterfly computations including performing a second plurality of intermediate butterfly computations simultaneously in parallel.

14. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 13, wherein:

the step of performing a second plurality of intermediate butterfly computations simultaneously in parallel including performing at least four intermediate butterfly computations simultaneously in parallel.

15. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 1, wherein:

the step of shifting the input coefficients left a plurality of bits including shifting the input coefficients left at least 4-bits.

16. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 1, further comprising:

loading the input coefficients into at least one register including loading a plurality of the input coefficients simultaneously in parallel and shifting the input coefficients left a plurality of bits prior to the step of performing the first 1D IDCT.

17. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 16, wherein:

the step of loading a plurality of coefficients simultaneously in parallel including loading at least four coefficients simultaneously in parallel.

18. The method for performing the IDCT on the plurality of input coefficients as claimed in claim 1, wherein:

the step of shifting the input coefficients left including shifting a plurality of the input coefficients left simultaneously in parallel.

19. The method for performing the IDCT on the plurality of input coefficients as

claimed in claim 18, wherein:

the step of shifting a plurality of the coefficients left simultaneously including shifting at least four coefficients simultaneously in parallel.

20. A method for performing an inverse discrete cosine transform (IDCT) on a plurality of input coefficients, the method for performing the IDCT comprising:

performing a first one directional (1D) IDCT resulting in a plurality of first 1D IDCT coefficients including utilizing a round-near-positive (RNP) rounding scheme;

performing a second 1D IDCT resulting in a plurality of second 1D IDCT coefficients including utilizing a round-near-positive (RNP) rounding scheme; and

rounding and shifting the plurality of second 1D IDCT coefficients resulting in a plurality of output coefficients including rounding utilizing a round away from zero (RAZ) rounding scheme.

21. The method for performing the IDCT as claimed in claim 20, wherein:

the step of rounding and shifting including rounding utilizing the RAZ rounding scheme including:

shifting the second 1D IDCT final coefficient right a plurality of bits resulting in a shifted final coefficient;

adding a conditional constant with the shifted final coefficient resulting in a conditional product;

adding the second 1D IDCT final coefficient with the conditional product resulting in a compensated final product; and

shifting the compensated final product right a plurality of bits.

22. The method for performing the IDCT as claimed in claim 21, wherein:

the step of shifting the second 1D IDCT final coefficient including shifting the second 1D IDCT final coefficient right at least 15-bits.

23. The method for performing the IDCT as claimed in claim 21, wherein:

the step of adding the conditional constant including:

adding 32 if the second 1D IDCT final coefficient is positive; and

adding 31 if the second 1D IDCT final coefficient is negative.

24. The method for performing the IDCT as claimed in claim 21, wherein:

the step of shifting the compensated final product left including shifting the

compensated final product right at least 6-bits.

25. The method for performing the IDCT as claimed in claim 21, wherein:

the step of rounding and shifting including performing the step of rounding and shifting in four instructions.

26. The method for performing the IDCT as claimed in claim 25, wherein:

performing a plurality of the steps of rounding and shifting simultaneously in parallel.

27. The method for performing the IDCT as claimed in claim 20, wherein:

the step of rounding and shifting including performing at least four of the steps of rounding and shifting simultaneously in parallel.

28. The method for performing the IDCT as claimed in claim 20, further comprising:

transposing the first 1D IDCT coefficients prior to performing the second 1D IDCT; and

transposing the IDCT output coefficients resulting in final IDCT outputs coefficients.

29. The method for performing the IDCT as claimed in claim 28, further comprising:

the step of transposing the first 1D IDCT coefficients and the IDCT output coefficients including implementing a shuffle a instruction.

30. The method for performing the IDCT as claimed in claim 28, further comprising:

clipping the final IDCT outputs coefficients.

31. A method for decompressing compressed data having a plurality of input coefficients, comprising:

performing a first one directional (1D) IDCT and a second 1D IDCT on the plurality of input coefficients resulting in output coefficients including:

utilizing a round near positive (RNP) rounding scheme;

not utilizing a round away from zero (RAZ) rounding scheme; and

rounding and shifting the output coefficients including utilizing the RAZ rounding scheme.

32. The method for decompressing compressed data as claimed in claim 31, wherein:

the IDCT is performed in less than 397 cycles.

33. The method for decompressing compressed data as claimed in claim 32, wherein:

complying with an Institute of Electrical and Electronics Engineers (IEEE) 1180 accuracy standard.

34. The method for decompressing compressed data as claimed in claim 33, wherein:

implementing the IDCT utilizing single instruction multiple data instructions (SIMD).

35. The method for decompressing compressed data as claimed in claim 34, wherein:

performing at least four SIMD instructions simultaneously in parallel.

36. The method for decompressing compressed data as claimed in claim 31, wherein:

performing the first 1D IDCT and the second 1D IDCT such that four coefficients are operated on simultaneously in parallel.

37. An apparatus for decompressing a compressed data signal, comprising:

a means for loading a plurality of input coefficients into at least one register;

a means for shifting the input coefficients a plurality of bits coupled with the register configured to receive the input coefficients and produce shifted input coefficients;

a means for performing a first one directional (1D) Inverse Discrete Cosine Transform (IDCT) coupled with the means for shifting the input coefficients configured to receive the shifted coefficients and produce a first 1D IDCT output matrix;

a means for transposing the first 1D IDCT output matrix coupled with the means for performing the first IDCT configured to transpose the first 1D IDCT output matrix and to produce a first transposed IDCT output matrix;

a means for performing a second 1D IDCT on the transposed IDCT output

matrix coupled with the means for transposing the first IDCT output matrix configured to receive the transposed first IDCT output matrix and to produce a second IDCT output matrix;

a means for rounding away from zero (RAZ) and shifting coupled with the means for performing the second 1D IDCT configured to round and shift coefficients of the second 1D IDCT output matrix to produce rounded second 1D IDCT output matrix; and

a means for transposing the rounded second 1D IDCT output matrix coupled with the means for RAZ and shifting configured to transpose the rounded second 1D IDCT output matrix to produce a decompressed output.

38. The apparatus for decompressing a compressed data signal as claimed in claim 37, further comprising:

a microprocessor including parallel processing, multimedia applications, at least one register, the means for loading a plurality of input coefficients, the means for shifting the input coefficients, the means for performing a first 1D IDCT, the means for transposing the first 1D IDCT, the means for performing the second 1D IDCT, the means for RAZ and shifting, the means for transposing the rounded second 1D IDCT output matrix; and

the microprocessor configured to perform at least one single instruction multiple data (SIMD) instruction on a plurality of coefficients simultaneously in parallel.

39. A computer program product for providing the decompression of a compressed signal, the computer program product including a computer readable storage medium an a computer program mechanism embedded therein, the computer program mechanism comprising:

a method of performing an Inverse Discrete Cosine Transform (IDCT) comprising:

loading a plurality of input coefficients into at least one register;

shifting the input coefficients left a plurality of bits;

performing a first one directional (1D) Inverse Discrete Cosine

Transform (IDCT) including utilizing a round near positive (RNP) rounding scheme producing a first IDCT output matrix;

transposing the first IDCT output matrix producing a transposed IDCT output matrix;

performing a second 1D IDCT on the transposed IDCT output matrix including utilizing a RNP rounding scheme producing a second IDCT output matrix including a plurality of components;

rounding away from zero and shifting each of the components of the second IDCT output matrix producing a rounded IDCT output matrix; and

transposing the rounded IDCT output matrix producing a decompressed output.